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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/521,672	01/18/2005	Martin J. Edwards	GB02 0116 US	2325
24738	7590	11/13/2007		
PHILIPS ELECTRONICS NORTH AMERICA CORPORATION INTELLECTUAL PROPERTY & STANDARDS 370 W. TRIMBLE ROAD MS 91/MG SAN JOSE, CA 95131			EXAMINER CARTER III, ROBERT E	
			ART UNIT 2629	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/521,672

Applicant(s)

EDWARDS, MARTIN J.

Examiner

Robert E. Carter

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 September 2007.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application
- ☐ Other: _____

DETAILED ACTION

Response to Amendment

1. The amendment filed on 09/12/2007 has been entered and considered by the examiner.

Information Disclosure Statement

2. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609.04(a) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Please include the following references from the specification in an IDS statement to make the record clear:

The references listed below should be provided so that they can be considered.

WO 02/063387

R. Greene et al "Manufacturing of Large Wide-View angle Seamless Tiled AMLCDs for Business and Consumer Applications", IDMC 2000, pages 191-194.

UA-A-5130829

Takeda et al "Simplified Method of Capacitively Coupled Driving for TFT-LCD" published in Proc. Japan Display 89, pages 580 – 583.

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T. Kamiya et al "A Novel Driving Method of TFT-LCD with Low Power Consumption" published in Proc. A MLCD '94, Tokyo, pages 60 62.

WO 03/014808

Please include copies of any of the above references per 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

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4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bae et al. (US Patent # 6,256,076) in view of Greene et al. (US Patent # 6,667,783).

As for claim 1, Bae et al. (Fig. 24) discloses:

An active matrix liquid crystal display device having an array of picture elements (Fig. 24), each comprising a picture element electrode (CLC) and a switching device (Q), located at respective intersections between crossing sets of selection (GL) and data (DL) address conductors connected to the picture elements, wherein each picture element includes a storage capacitor (CST) connected between the picture element electrode and a capacitor line (line of storage capacitors CST connected in a row) shared by the picture elements in the same row, and wherein the selection address conductor associated with one row of picture elements is coupled to the capacitor line associated with a different row of picture elements (the left end of the capacitor lines are connected to the previous gate lines).

Bae et al. does not teach a set of connection lines supplying signals to the selection address conductors.

In the same field of endeavor (i.e. LCD structures) Greene et al. (Fig. 9c) discloses:

a set of connection lines (200) for supplying selection signals to the set of selection address conductors (186), which connection lines extend from one side of the array

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(Access Side) in the direction of the set of data address conductors (182) and are connected (210) to respective ones of the set of selection address conductors,

combining Bae et al. and Greene et al. would meet the claimed limitations:

wherein the selection address conductor associated with one row of picture elements is coupled to the capacitor line associated with a different row of picture elements so that each connection line is connected to a respective selection address conductor for one row of picture elements and its coupled capacitor line for another row of picture elements.

Since Bae et al. teaches selection address conductors coupled to capacitor lines and Greene et al. teaches connection lines connected to selection address conductors the obvious combination of the references teaches connection lines connected to selection address conductors and capacitor lines.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the display device of Bae et al. by adding the connecting lines of Greene et al. to improve sharpness, contrast, and display form factor (Greene et al., Col. 7, lines 12-18).

As for claim 2, Bae et al. teaches:

wherein the selection address conductor associated with one row of picture elements is coupled to the capacitor line associated with an adjacent row of picture elements (the left end of the capacitor lines are connected to the previous gate lines).

As for claim 3, Bae et al. teaches:

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wherein a selection address conductor and a capacitor line are coupled by an interconnection between their ends at one side of the array (the left end of the capacitor lines are connected to the previous gate lines).

As for claim 4, Bae et al. as modified by Greene et al. teaches the limitations of claim 1.

Bae et al. as modified by Greene et al. does not teach:
wherein the interconnections for successive selection address conductors and their respective associated capacitor lines are arranged alternately at opposite sides of the array.

However, the display device defined by the limitations of claim 4 is electrically equivalent to the display device of Bae et al. as modified by Greene et al. as used in the rejection of claim 1 above. Therefore the limitations of claim 4 are simply that of design choice, and at the time of the invention making such design choices would have been obvious to one of ordinary skill in the art to do so as to optimize circuit layout for manufacturing of the display device.

Yasui (US Patent # 4,822, 142) discloses an exemplary LCD display with interconnections of selection address conductors arranged alternately at opposite sides of the array (the conductors are connected to the next conductor inside the drivers 17 and 17')

As for claim 5, Greene et al. teaches:
wherein each connection line (200) extends from one side of the array (Access Side) and is connected at a connection point (210) to the selection address conductor (186)

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with which it is associated that is closest to that side, and wherein the connection line terminates at that connection point.

As for claim 7, Bae et al. teaches:

wherein the picture element array is driven using a capacitively coupled drive scheme in which part of the drive voltage applied to the picture element electrode is provided via the storage capacitor (Fig. 12, Col. 9, lines 24-33, The storage capacitor is charged when driving and maintains the drive voltage on the pixel).

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bae et al. in view of Greene et al. as applied to claims 1-5, and 7 above, and further in view of Fujikawa et al. (US Patent # 5,995,177).

As for claim 6, Bae et al. as modified by Greene et al. teaches the limitations of claim 1.

Bae et al. as modified by Greene et al. does not teach the capacitor line and selection address conductor of a row of picture elements extending along opposite sides of the row.

In the same field of endeavor (i.e. LCD displays with capacitor lines) Fujikawa et al. discloses:

wherein the capacitor line (3) and selection address conductor (2) associated with one row of picture elements extend along opposite sides of the row of picture elements

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the selection address conductors and capacitor

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lines of Bae et al. as modified by Greene et al. with the layout of the ones in Fujikawa et al. to reduce manufacturing steps while maintaining satisfactory contact points (Fujikawa et al., Col. 5, lines 23-30).

Response to Arguments

8. Applicant's arguments, see page 5, line 19 – page 6, line 2, and page 6, line 21 – page 7, line 1, filed 09/12/2007, with respect to the rejection(s) of claim(s) 1-5 under 35 U.S.C 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Bae et al., which discloses a capacitor line for each row connected at one end to the previous gate line.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Yasui (US Patent # 4,822, 142) discloses an LCD display with interconnections of selection address conductors arranged alternately at opposite sides of the array.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Carter whose telephone number is 571-270-3006. The examiner can normally be reached on M-F.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on 571-272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

REC


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SUPERVISORY PATENT EXAMINER